WHAT IS CLAIMED IS:

1. A memory device comprising:

a data memory to and from which data is input and output via a data bus for a data memory; and

a plurality of buffer circuits for inputting and outputting data to and from said data memory via a first data bus that has a bus width the same as that of the data bus for said data memory and that is electrically connected to the data bus for said data memory, and inputting and outputting data to and from a data processing circuit via a second data bus having a bus width smaller than that of the data bus for said data memory.

2. The device according to claim 1, further comprising a selector, which is connected between said plurality of buffer circuits and said data memory, for allowing input/output of data between any one of said plurality of buffer circuits and said data memory.

3. The device according to claim 1, wherein the bus width of the second data bus is a fraction of that of the bus for said data memory.

4. The device according to claim 1, wherein the data input and output between said data memory and said plurality of buffer circuits is image data, and said device further comprises an arbitration circuit for

controlling the plurality of buffer circuits in such a manner that image data representing images of different frames is input and output to and from different buffer circuits in a common time period.